

Application Number 10/657,867
Amendment dated October 25, 2006

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REMARKS

The applicants thank Examiners Lewis and Wilczewski for their helpful and thoughtful comments during the telephone interviews conducted with the undersigned on August 16, 2006 and August 21, 2006. The applicants also appreciate the Examiners' time spent in reviewing a draft of the present Amendment prior to filing the Amendment, and providing comments regarding the Amendment during the telephone interview of September 12, 2006.

The drawings are objected to under 37 C.F.R. 1.83(a). The specification and claims are amended to clarify the present invention. In the present invention, a first insulating layer is formed on the semiconductor substrate 10, and a silicon layer is formed thereon. Thereafter, the silicon layer is dry etched to form silicon layer patterns 34 on both sides of the exposed collector region 16 over the isolation regions 20, and the first insulating layer is wet etched using the silicon layer patterns 34 as an etch mask to form first insulating layer patterns 32 on both sides of the exposed collector region 16 over the isolation regions 20, as shown in Figure 2. A first base semiconductor layer is then formed on the resultant structure. The specification is amended to clarify that first and second silicon layer patterns 34 are formed and that first and second insulating layer patterns 32 are formed, as shown in Figure 2. The drawings and the specification clearly support that the insulating layer patterns 32 are portions of a single layer and the silicon layer patterns 34 are portions of a single layer (see the specification as filed at least at page 6, line 26 through page 7, line 5 and Figure 2 as filed). In addition, the drawings and the specification clearly support that the first insulating layer patterns 32 and the silicon layer patterns 34 are formed on both sides of the exposed collector region (see the specification as filed at least at page 6, lines 26-29 and Figure 2). No new matter is added by the clarifying amendments.

The claims are amended to recite that first and second insulating layer patterns are formed between the first and second isolation layers, respectively, and the first base semiconductor layer, under the base electrode. Figure 12 clearly discloses insulating

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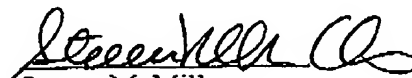
layer patterns 32 formed on both sides of the collector region 16 between the isolation regions 20 on both sides of the collector region 16 and the first base semiconductor layer 40, under the base electrodes 82. The claims are further amended to recite that first and second silicon layer patterns are formed between the first and second insulating layer patterns, respectively, and the first base semiconductor layer. Figure 12 clearly shows silicon layer patterns 34 formed on both sides of the collector region 16 between the insulating layer patterns 32 on both sides of the collector region 16 and the first base semiconductor layer 40. Therefore, no new matter is added by the claim amendments. Therefore, it is believed that the objection to the drawings is overcome, and reconsideration thereof is requested.

Further, the claims and specification are amended to clarify that the second base semiconductor layers 60 include a pattern, as shown at least at Figure 8 and described in the specification as filed at least at page 8, lines 8-13. The claims and specification are further amended to clarify that the base ohmic layers 70 include a pattern, as shown at least at Figure 9 and described in the specification as filed at least at page 8, lines 14-22.

In view of the foregoing amendments and remarks, it is believed that all claims pending in the application (claims 21-28) are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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